

TARDIS (Time and Remanence Decay In SRAM):

Secure Time Keeping For Embedded Devices Without Clocks

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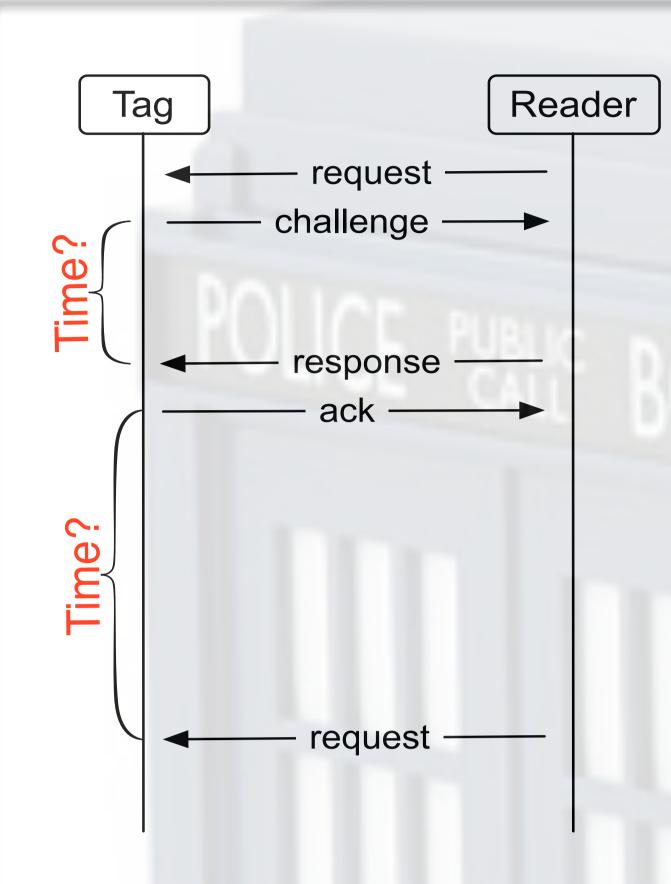
UMass Amherst

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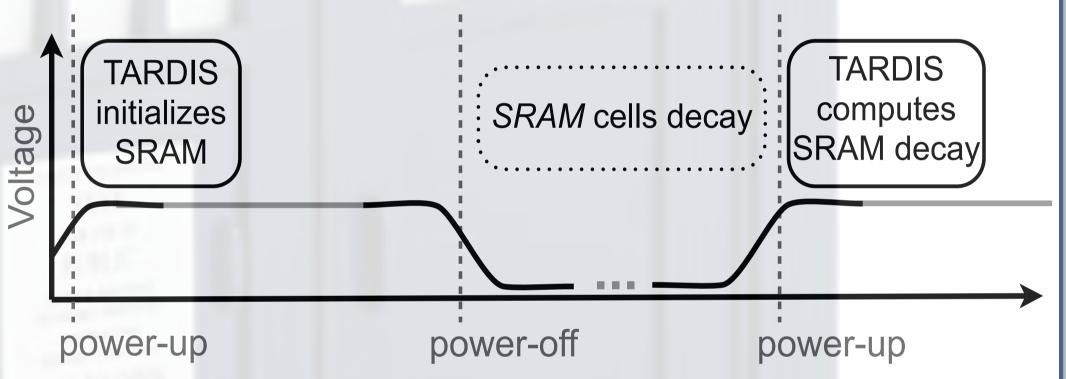
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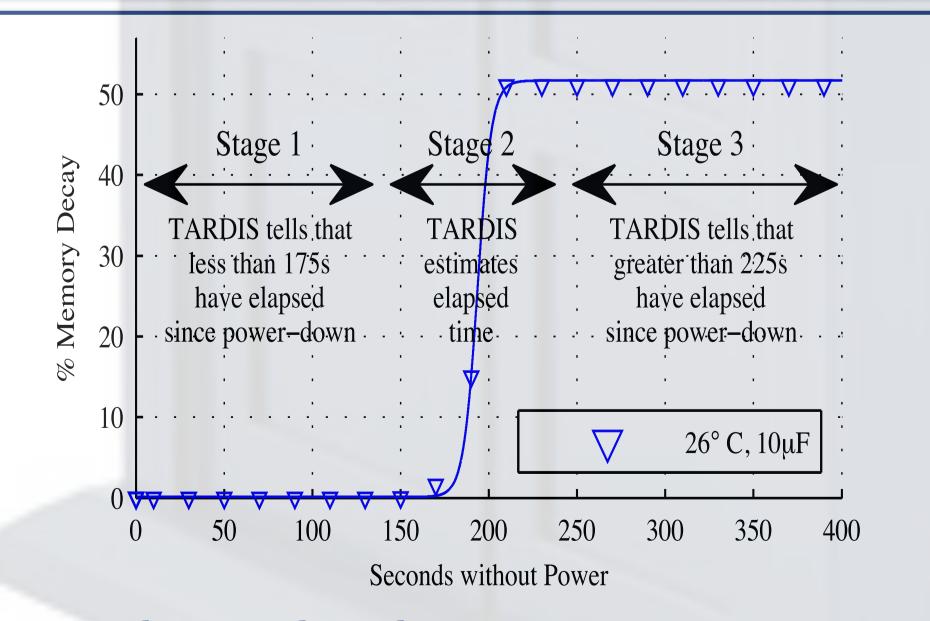
- Smart cards, RFID tags and other intermittently powered devices do not have a notion of time across power ups.
- Lack of a trustworthy clock makes it difficult to implement security protocols.
- Any solution must consider legacy hardware and implementations costs.



SRAM is a **volatile memory** that loses data in the absence of power. This loss of data is gradual and depends on the circuit's specifications, capacitance, and temperature. TARDIS derives a notion of time from the gradual data loss.



TARDIS works by first initializing a portion of **SRAM to 1's**. After a power loss, TARDIS reads the **SRAM** and will use the **decay percentage** (ratio of flipped bits) and the reading from the temperature sensors present in these devices to maintain a sense of time elapsed.



Estimated power loss duration on a TI MSP430F2131

Time frames can be tweaked based on cap size from few seconds to hours

Applications

• Preventing brute force attacks:

Platform	# Queries
Mifare Classic	>1500
Mifare DESfire	250,000
UHF RFID tags	200
TI DST	~75,000
GSM SIM Card	150,000

- Allowing time-out in security protocols
- Preventing Passback and Double Reads
- Implementing E-coupons

